FIG 1

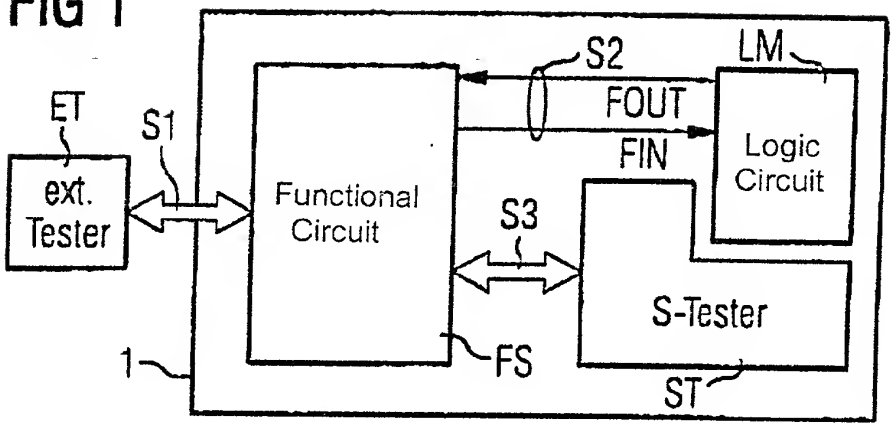
ET
S1
ext.
Tester
Functional
Circuit
S2
FOUT
FIN
LM
Logic
Circuit
S3
S-Tester
1
FS
ST

FIG 2

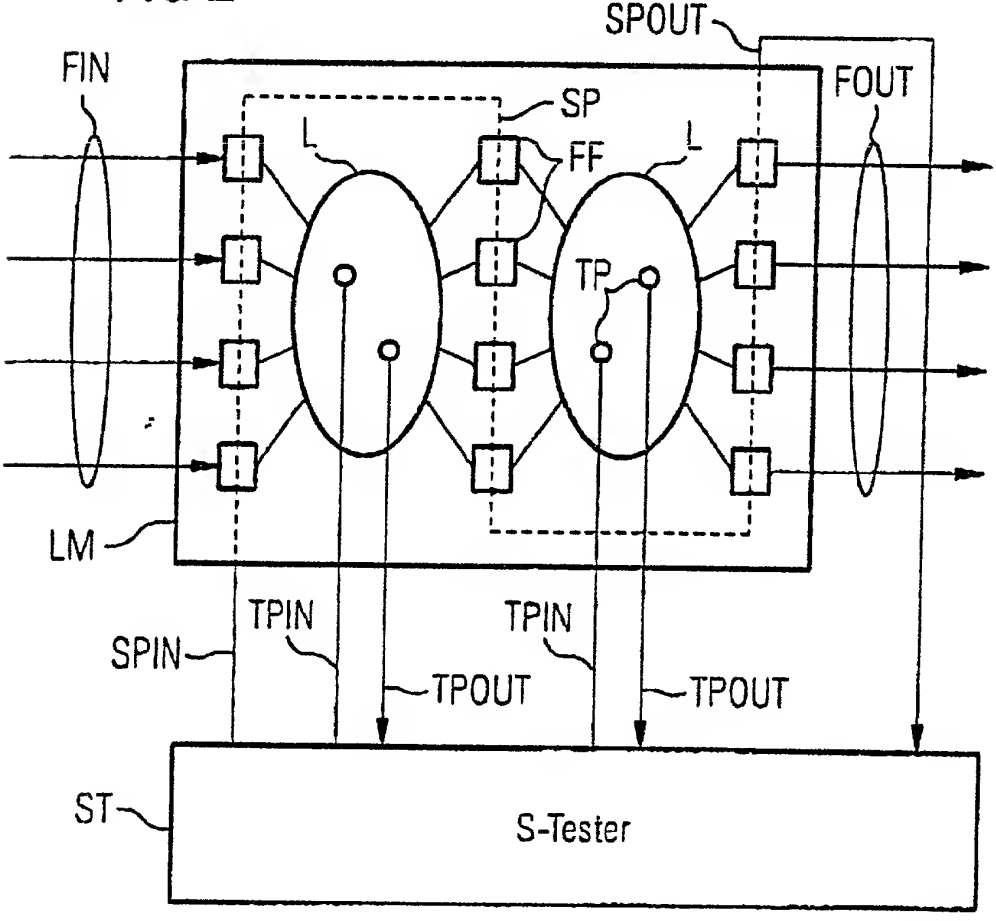
SPOUT
FIN
FOUT
SP
L
FF
L
TP
LM
TPIN
TPIN
SPIN
TPOUT
TPOUT
ST
S-Tester

FIG 3

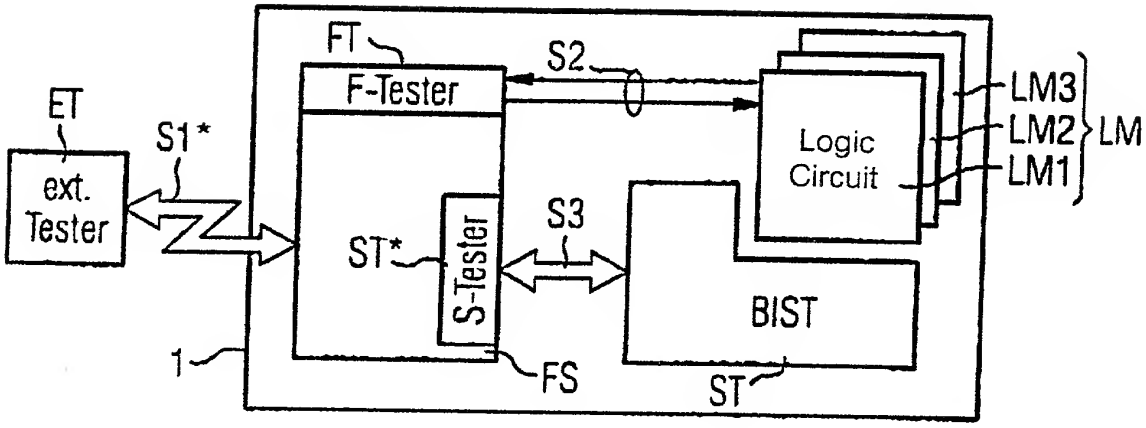
FT
F-Tester
S2
ET
S1*
ext.
Tester
ST*
S-Tester
S3
Logic
Circuit
LM3
LM2
LM1
LM
BIST
1
FS
ST

FIG 4 PRIOR ART

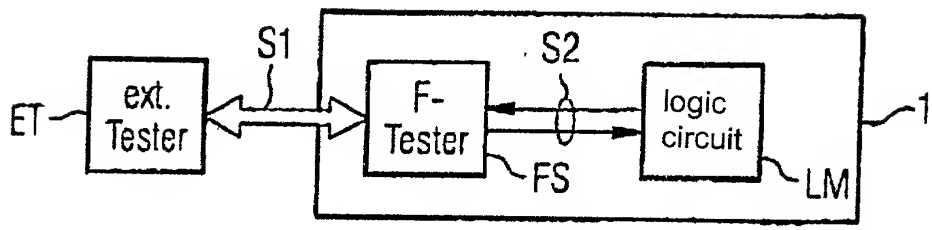

FIG 5 PRIOR ART

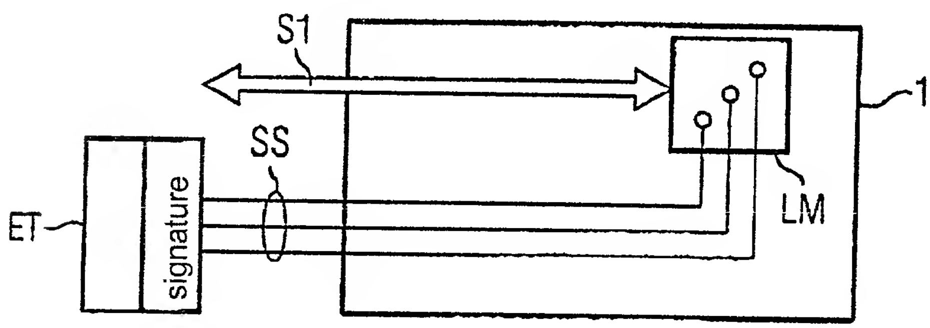

FIG 6 PRIOR ART